PIC16F13145 Family Full-Featured 8/14/20-Pin Microcontrollers

PIC16F13145 Family

Introduction

The PIC16F13145 microcontroller family, with its focused set of peripherals, provides an effective method to implement hardware-based solutions.

This device family introduces the Configurable Logic Block (CLB) peripheral, enabling users to incorporate hardware-based custom logic into their applications. The CLB is comprised of 32 individual logic elements. Each logic element's Look Up Table (LUT) based design offers vast customization options, and CPU-independent operation improves the response time and power consumption.

This product family is available in 8, 14, and 20-pin packages and offers up to 14 KB of Program Flash Memory with up to 1 KB of RAM. Along with the CLB, the product family offers a 10-bit Analog to Digital Converter with Computation (ADCC) capable of up to 100 ksps; an 8-bit Digital to Analog Converter; two fast Comparators (50 ns response time); and a collection of other peripherals for timing control and serial communications with SMBus compatibility.

The small form factor, combined with the CLB and other core independent peripherals, makes the PIC16F13145 family well-suited for various applications such as real-time control, digital sensor nodes, and market segments such as industrial and automotive.

PIC16F13145 Family Summary

Table 1. Devices Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	32-Bit CRC with NVM Scanner	I/O Pins(1)/ Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timers(2)	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	I2C/SPI	EUSART	CLB	CLC	FVR	CMP	8-bit DAC	SMBus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Windowed Watchdog Timer
PIC16F13113	3.5k	256	Y/Y	Y	6/Y	1/1	2/2	5/5	1/1	1	1	4	2	2	1	Y	1	6	Y
PIC16F13114	7k	512	Y/Y	Y	6/Y	1/1	2/2	5/5	1/1	1	1	4	2	2	1	Y	1	6	Y
PIC16F13115	14k	1024	Y/Y	Y	6/Y	1/1	2/2	5/5	1/1	1	1	4	2	2	1	Y	1	6	Y
PIC16F13123	3.5k	256	Y/Y	Y	12/Y	1/1	2/2	11/5	1/1	1	1	4	2	2	1	Y	1	12	Y
PIC16F13124	7k	512	Y/Y	Y	12/Y	1/1	2/2	11/5	1/1	1	1	4	2	2	1	Y	1	12	Y
PIC16F13125	14k	1024	Y/Y	Y	12/Y	1/1	2/2	11/5	1/1	1	1	4	2	2	1	Y	1	12	Y
PIC16F13143	3.5k	256	Y/Y	Y	18/Y	1/1	2/2	17/5	1/1	1	1	4	2	2	1	Y	1	18	Y
PIC16F13144	7k	512	Y/Y	Y	18/Y	1/1	2/2	17/5	1/1	1	1	4	2	2	1	Y	1	18	Y
PIC16F13145	14k	1024	Y/Y	Y	18/Y	1/1	2/2	17/5	1/1	1	1	4	2	2	1	Y	1	18	Y

Notes:

1. Total I/O count includes one pin ($\overline{MCLR}$) that is input-only.
2. Timer0 can be configured as either an 8-bit or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC-32 MHz clock input
  - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- Windowed Watchdog Timer (WWDT)

Memory

- Up to 14 KB of Program Flash Memory
- Up to 1 KB of Data SRAM Memory
- Memory Access Partition (MAP) with Program Flash Memory Partitioned into:
  - Application block
  - Boot block
  - Storage Area Flash (SAF) block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Fixed Voltage Reference (FVR) measurement data
  - Temperature Indicator calibration coefficients
  - Microchip Unique Identifier (MUI)
- Device Characteristics Information (DCI) Stores:
  - Program/erase row sizes
  - Pin count details
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep:
  - Lowest power consumption
  - Reduce system electrical noise while performing ADC conversions
- Low Power Mode Features:
  - Sleep:
    - < 900 nA typical @ 3V/25°C (WDT enabled)
    - < 600 nA typical @ 3V/25°C (WDT disabled)
  - Operating Current:
    - 48 µA typical @ 32 kHz, 3V/25°C
    - < 1 mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- One Configurable Logic Block (CLB)
  - Interconnected fabric containing 32 Basic Logic Elements (BLE)
    - Each BLE contains one 4-input Look-Up Table (LUT) and one flip-flop
    - Schematically programmable using MPLAB Code Configurator
  - Dedicated 3-bit hardware counter
- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Two Pulse-Width Modulators (PWM):
  - 10-bit resolution
- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Configurable 8/16-Bit Timer (TMR0)
- One 16-Bit Timer (TMR1) with Gate Control
- One 8-Bit Timer (TMR2) with Hardware Limit Timer (HLT)
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- One Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485, LIN compatible
  - Auto-wake-up on Start

- One Host Synchronous Serial Port (MSSP):
  - Serial Peripheral Interface (SPI) mode
    - Chip Select Synchronization
  - Inter-Integrated Circuit (I^2C) mode
    - 7/10-bit Addressing modes
    - SMBus support
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Device I/O Port Features:
  - Up to 17 I/O pins
  - Individual I/O direction, open-drain, input threshold, slew rate and weak pull-up control
  - Interrupt-on-Change (IOC) on all pins
  - One external interrupt pin

Analog Peripherals

- Single-ended Analog-to-Digital Converter with Computation (ADCC):
  - Sample rate up to 100 ksps
  - 10-bit resolution
  - Up to 17 external input channels
  - Five internal input channels
  - Internal ADC oscillator (ADCRC)
  - Operates in Sleep
  - Selectable auto-conversion trigger sources
- One 8-Bit Digital-to-Analog Converter (DAC):
  - Buffered output available on up to two I/O pins
  - Internal connections to ADC and Comparators
- Two Comparators (CMP):
  - Configurable power modes for faster response time (50ns) or lower power operation
  - Up to four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Two Fixed Voltage References (FVR):
  - Selectable 1.024V, 2.048V and 4.096V output levels
  - FVR1 internally connected to ADC
  - FVR2 internally connected to Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 32 MHz
  - ±2% at calibration
- Internal 31 kHz Oscillator (LFINTOSC)
- External High-Frequency Clock Input:
  - Three Crystal/Resonator modes
  - Two External Clock (EC) Power modes
  - 4xPLL available for external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if the external clock source stops
- Oscillator Start-up Timer (OST):
  - Ensures the stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip