AVR64DU28/32 Preliminary Data Sheet

AVR64DU28/32

Introduction

The AVR® DU Family of microcontrollers uses the AVR® CPU with a hardware multiplier running at clock speeds up to 24 MHz. They include 16/32/64 KB of Flash, 2/4/8 KB of SRAM, and 256 bytes of EEPROM. The microcontrollers are available in 14-, 20-, 28-, and 32-pin packages. The family uses the latest technologies from Microchip Technology, with a flexible and low-power architecture, including an Event System, intelligent analog features, and advanced digital peripherals such as a USB 2.0 full-speed device.

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Features

- AVR® CPU
  - Running at up to 24 MHz
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Program and Debug Interface Disable (PDID)
  - Supply voltage range: 1.8-5.5V
- Memories
  - 16/32/64 KB in-system self-programmable Flash memory with a genuine read-while-write operation
  - 2/4/8 KB SRAM
  - 256B EEPROM
  - 512B of user row in nonvolatile memory that can keep data during chip erase and be programmed while the device is locked
  - 256B of boot row
  - Write/erase endurance
    - Flash 1,000 cycles
    - EEPROM 100,000 cycles
  - Data retention: 40 years at 55°C
- System
  - Power-on Reset (POR) circuit
  - Brown-out Detector (BOD)
  - Voltage Level Monitor (VLM) with interrupt at a programmable level above the BOD
  - Clock options
    - High-precision internal high-frequency oscillator with selectable frequency up to 24 MHz (OSCHF)
      - Auto-tuning for improved internal oscillator accuracy
    - 32.768 kHz internal oscillator (OSC32K)
    - 32.768 kHz external crystal oscillator (XOSC32K)
    - External clock input
    - External high-frequency crystal oscillator (XOSCHF) with clock failure detection
  - Single-pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle with all peripherals running for immediate wake-up
    - Standby with a configurable operation of selected peripherals
    - Power-Down with full data retention
  - Automated Cyclic Redundancy Check (CRC) Flash memory scan
  - Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
  - External interrupt on all general purpose pins
- Peripherals
  - One 16-bit Timer/Counter type A (TCA) with three compare channels for Pulse-Width Modulation (PWM) and waveform generation

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  - Two 16-bit Timer/Counter type B (TCB) with input capture and signal measurements
  - One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator
  - One USB 2.0 full-speed (12 Mbps) device-compliant interface[(1)]
    - Optional internal 3.3V voltage regulator
    - OSCHF oscillator can be tuned to the USB Start-of-Frames (SOFs) for crystal-less operation
    - 16 endpoint addresses each, with one input and one output endpoint for up to 32 endpoints
    - Multipacket transfer for reduced interrupt load and software intervention
  - Two USARTs
    - Operation modes: RS-485, LIN client, SPI host, and IrDA
    - Fractional baud rate generator, auto-baud, and start-of-frame detection
  - One SPI with host/client operation modes
  - One Two-Wire Interface (TWI) with dual address match
    - Simultaneous host/client operation (dual mode)
    - Philips Inter-Integrated Circuit (I^2C) compatible
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)[(2)]
  - Event System for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with four programmable Look-up Tables (LUTs)
  - One 10-bit 170 ksps Analog-to-Digital Converter (ADC)
  - One Analog Comparator (AC)
  - Internal 1.024V, 2.048V, 2.500V and 4.096V voltage references and external reference option (VREF)
- I/O and Packages:
  - Up to 25 (24) programmable GPIO (I/O) pins
  - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
  - 28-pin VQFN 4x4 mm, SPDIP and SSOP
  - 20-pin VQFN 3x3 mm and SSOP
  - 14-pin SOIC
- Temperature Ranges:
  - Industrial: -40°C to +85°C

Notes:

1. USB function is only available for VDD above 3.0V.
2. I^2C Fm+ is only supported for 2.7V and above.

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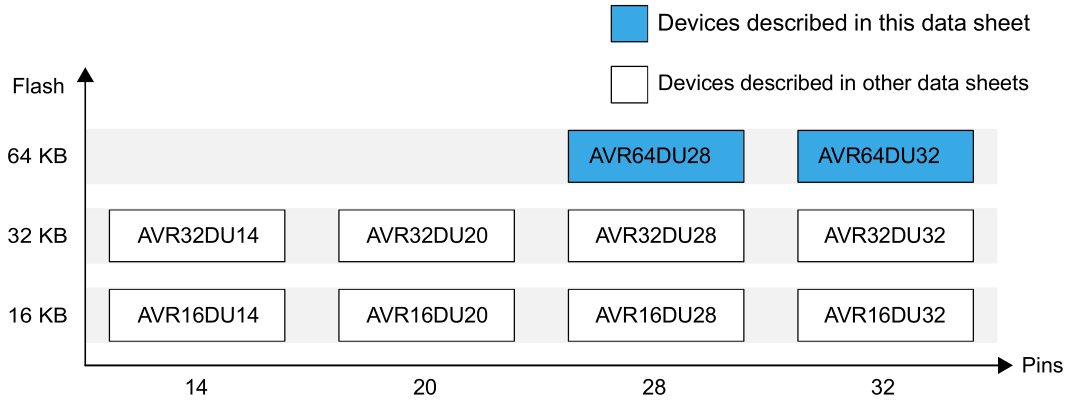
AVR® DU Family Overview

The figure below shows the AVR DU devices, laying out pin count variants and memory sizes:

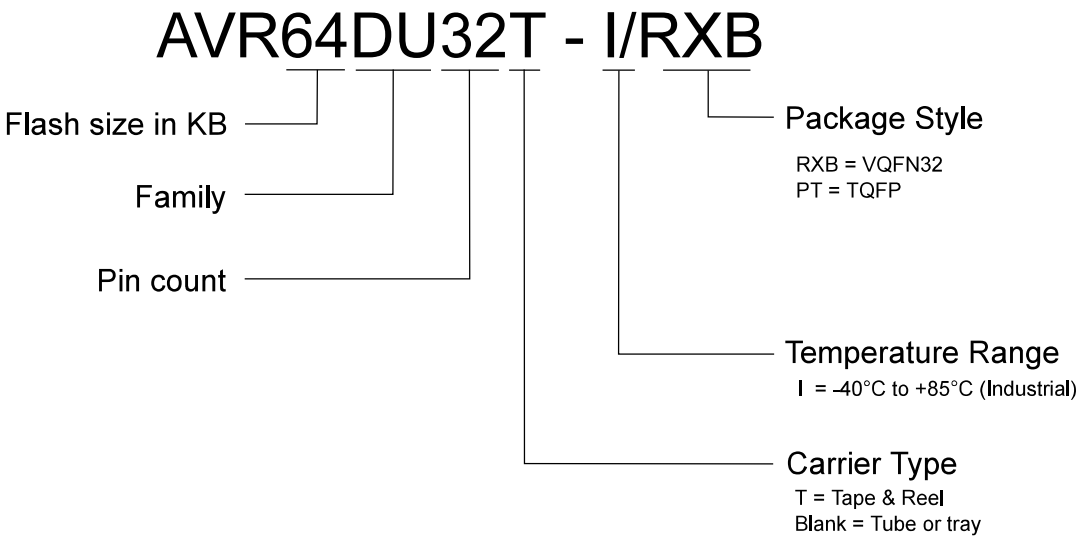
- Vertical migration is possible without code modification, as these devices are entirely pin and feature compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. AVR® DU Family Overview



The name of a device in the AVR DU Family is decoded as follows:

Figure 2. AVR® DU Device Designations



Memory Overview

The following table shows the memory overview of the entire AVR DU family.

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Table 1. Memory Overview

Devices	AVR16DU14 AVR16DU20 AVR16DU28 AVR16DU32	AVR32DU14 AVR32DU20 AVR32DU28 AVR32DU32	AVR64DU28 AVR64DU32
Flash memory	16 KB	32 KB	64 KB
Flash read-while-write sectioning - bottom NRWW /upper RWW	4 KB/12 KB	4 KB/28 KB	8 KB/56 KB
SRAM	2 KB	4 KB	8 KB
EEPROM	256B	256B	256B
User row	512B	512B	512B
Boot row	256B	256B	256B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR DU family.

Table 2. Peripheral Overview

Feature	AVR16DU14 AVR32DU14	AVR16DU20 AVR32DU20	AVR16DU28 AVR32DU28 AVR64DU28	AVR16DU32 AVR32DU32 AVR64DU32
Pins	14	20	28	32
Max. frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	1	1
16-bit Timer/Counter type B (TCB)	2	2	2	2
Real-Time Counter (RTC)	1	1	1	1
USB 2.0 full-speed device	1	1	1	1
USART	2	2	2	2
SPI	1	1	1	1
TWI/I^2C[1]	1[1]	1[1]	1[1]	1[1]
10-bit ADC (channels)	1 (5)	1 (11)	1 (17)	1 (21)
Analog Comparator (AC)	1	1	1	1
Peripheral Touch Controller (PTC)	-	-	-	-
Operational amplifier (OP)	-	-	-	-
Configurable Custom Logic Look-up Table (CCL LUT)	4	4	4	4
Watchdog Timer (WDT)	1	1	1	1
Event System (EVSYS) channels	6	6	6	6
General Purpose I/O[2]	9/8[2]	15/14[2]	21/20[2]	25/24[2]
PORT	PA[1:0], PC[3], PD[7:4], PF[7:6]	PA[7:0], PC[3], PD[7:4], PF[7:6]	PA[7:0], PC[3], PD[7:0], PF[7,6,1,0]	PA[7:0], PC[3], PD[7:0], PF[7:0]
External interrupts	9	15	21	25
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Notes:

1. The TWI/I^2C can operate simultaneously as both host and client on different pins.
2. PF6/$\overline{\text{RESET}}$ pin is input only.

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Security Concept

The AVR DU devices are general purpose microcontrollers that offer fundamental security features to implement secure firmware upgrades and authenticate the application firmware. When using the security features correctly, they protect against remote attacks and some PCB-level attacks where the application code is attempted modified to change the product functionality.

The cornerstone of the security features is the *Program and Debug Interface Disable (PDID)*, a mechanism preventing access to the device's reprogrammable Flash memory over the Unified Program and Debug Interface (UPDI). After activating the PDID as described in the section *Memories*, the UPDI is prevented from making any changes to the device. The UPDI can still read out the device information and CRC status.

The only way to program the device after activating the PDID is by using software stored in the Boot Code section of the Flash to update the Application Code section software. This application-specific software must be able to receive new data and program the Application Code section. It is impossible to alter code stored in the Boot Code section using this mechanism, as the Boot Code section is only accessible using the UPDI.

In addition, there is a separate storage space accessible only by code in the Boot Code section, which can hold any data intended to be accessible only from the Boot Code section. One example of this is a cryptographic key to be used to validate data that are sent to a bootloader to update the application software on the device.

This creates a two-layer security: The device is prevented from being erased or reprogrammed over the UPDI, and the code in the Boot Code section is protected. Secondly, the code in the Boot Code section can use a cryptographic key (that is only accessible by code in this section of Flash) to verify that any new application code that is received for the device software update is authentic.

Using the *Program and Debug Interface Disable (PDID)* in software requires cryptographic competencies to ensure conformity to cyber-security standards such as ISO/SAE DIS 21434.

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