ATtiny202/204/402/404/406

tinyAVR® 0-series

Introduction

The ATtiny202/204/402/404/406 are members of the tinyAVR® 0-series of microcontrollers, using the AVR® processor with hardware multiplier, running at up to 20 MHz, with 2/4 KB Flash, 128/256 bytes of SRAM, and 64/128 bytes of EEPROM in a 8-, 14-, or 20-pin package. The tinyAVR® 0-series uses the latest technologies with a flexible, low-power architecture, including Event System, accurate analog features, and Core Independent Peripherals (CIPs).

Attention: This data sheet is valid for industrial qualified devices.

Features

- CPU
  - AVR® CPU
  - Running at up to 20 MHz
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
- Memories
  - 2/4 KB In-system self-programmable Flash memory
  - 64/128 bytes EEPROM
  - 128/256 bytes SRAM
  - Write/erase endurance:
    - Flash 10,000 cycles
    - EEPROM 100,000 cycles
  - Data retention:
    - 40 years at 55°C
- System
  - Power-on Reset (POR)
  - Brown-out Detector (BOD)
  - Clock options:
    - 16/20 MHz low-power internal RC oscillator
    - 32.768 kHz Ultra Low-Power (ULP) internal RC oscillator
    - External clock input
  - Single-Pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes:
    - Idle with all peripherals running for immediate wake-up
    - Standby
      - Configurable operation of selected peripherals

    - Power-Down with full data retention
- Peripherals
  - One 16-bit Timer/Counter type A (TCA) with a dedicated period register and three compare channels
  - One 16-bit Timer/Counter type B (TCB) with input capture
  - One 16-bit Real-Time Counter (RTC) running from an external clock or internal RC oscillator
  - Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
  - One USART with fractional baud rate generator, auto-baud, and start-of-frame detection
  - One host/client Serial Peripheral Interface (SPI)
  - One Two-Wire Interface (TWI) with dual address match
    - Philips I^2C compatible
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)
  - One Analog Comparator (AC) with a low propagation delay
  - One 10-bit 115 ksps Analog-to-Digital Converter (ADC)
  - Multiple voltage references (V_{REF}):
    - 0.55V
    - 1.1V
    - 1.5V
    - 2.5V
    - 4.3V
  - Event System (EVSYS) for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with two programmable look-up tables
  - Automated CRC memory scan
  - External interrupt on all general purpose pins
- I/O and Packages:
  - Up to 18 programmable I/O lines
  - 8-pin SOIC150
  - 14-pin SOIC150
  - 20-pin SOIC300
  - 20-pin VQFN 3x3 mm
- Temperature Ranges:
  - -40°C to 105°C
  - -40°C to 125°C
- Speed Grades:
  - 0-5 MHz @ 1.8V – 5.5V
  - 0-10 MHz @ 2.7V – 5.5V
  - 0-20 MHz @ 4.5V – 5.5V